REMARKS

Applicant hereby corrects idiomatic and typographical errors in the specification as originally filed. Please see page 3, lines 9-12 and page 4, lines 1-4. Further, Applicants amended claims 13, 20, 29, and 42-45 to further clarify the claimed invention to facilitate the processing of this application. Also, a description regarding FIG. 6 has been added for better understanding of the application. No new matter has been added.

The Examiner is requested to call the undersigned if any questions arise concerning the above-mentioned application.

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.

Alan T. McCollom
Reg. No. 28,881

MARGER JOHNSON & McCOLLOM, P.C.
1030 SW Morrison Street
Portland, OR 97205
(503) 222-3613

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the specification

On page 9, lines 13-22

According to one aspect of the present invention, a crystallization temperature can be [lowered] increased forming the high-k dielectric layer 14 comprising one or more pairs of, alternating first layer 18 formed, for example, of HfO_2, Ta_2O_3, Y_2O_3 or ZrO_2 and second layer 22 formed, for example, of Al_2O_3 as illustrated in FIGS. 1B, 1C, and 2.

Preferably, the thicknesses of the first and second layers 18, 20 are in the range of approximately 2 to approximately 60 angstroms (critical thickness). More preferably, the thicknesses of the first and second layers are approximately 10 and 5 angstroms, respectively. It is contemplated that if the thicknesses of the first and second layers 18, 20 are within this range, the crystallization temperature can be [lowered] increased as compared to a bulk dielectric layer.

On page 9, line 29 – page 10, line 4

But, with the high-k dielectric layer 14 described above in accordance with the present invention, the crystallization temperature of the high-k dielectric layer 14 can be [reduced] increased compared to the prior art, thus reducing leakage current. Here, 2 angstroms is a basic thickness of one atomic layer, and 60 angstroms represents an upper thickness limit that prevents a popping phenomenon during a subsequent annealing process. As is known in the art, hydroxyl radicals trapped in dielectric layers during the formation can pop therefrom upon subsequent annealing, thereby damaging, e.g. leaving a hole in the dielectric layers. If such a popping phenomenon occurs, subsequent processing steps such as gate poly deposition can be significantly inhibited.

On page 11, lines 1-7

Further referring to FIG. 5, even though the amount of the flatband voltage shift is 0 volt, the transconductance of the MOS structure including the Al_2O_3 layer is still less than that of the reference MOS structure. This difference is due to the interface trap density. The interface trap density can be calculated using a charge pumping current shown in FIG. 6, which shows the charge pumping current of SiO_2 and Al_2O_3. As can be seen, the interface

trap density of Al_2O_3 is greater than SiO_2. Such interface trap density can be reduced by introducing the metal silicate interface layer 12 between the silicon substrate 10 and the high-k dielectric layer 14.

In the claims

19. (Amended) The multi-layer structure of claim 13, wherein the upper most layer of the high-k dielectric layer is Al_2O_3.

25. (Amended) The multi-layer structure of claim 20, wherein the upper most layer of the high-k dielectric layer is Al_2O_3.

30. (Amended) The method of claim 29, wherein the upper most layer of the high-k dielectric layer is Al_2O_3.

42. (Amended) A transistor comprising:
a substrate;
a silicate interface layer formed over the substrate; and
a high-k dielectric layer formed over the silicate interface layer;
a gate formed over the high-k dielectric layer; and
a source/drain region formed adjacent the gate.

45. (Amended) A capacitor for a semiconductor device, comprising;
a lower electrode;
a silicate interface layer formed over the lower electrode;
a high-k dielectric layer formed over the silicate interface layer; and
an upper electrode formed over the high-k dielectric layer.